

**What Is Claimed Is:**

- 1 1. A data recovery circuit, comprising:
  - 2 a clock generator for generating a first group of
  - 3 sampling clock pulses and a second group of sampling
  - 4 clock pulses for sampling an incoming data stream, each
  - 5 sampling edge of said first group of sampling clock
  - 6 pulses and each sampling edge of said second group of
  - 7 sampling clock pulses being arranged alternatively and
  - 8 being separated from each other for an interval equal
  - 9 to half the period of said incoming data stream, said
  - 10 clock generator being controlled in response to a phase
  - 11 control signal to adjust phases of said first group of
  - 12 sampling clock pulses and said second group of sampling
  - 13 clock pulses;
  - 14 a data and phase sampling circuit for receiving said
  - 15 incoming data stream, said first group of sampling clock
  - 16 pulses and said second group of sampling clock pulses,
  - 17 said data and phase sampling circuit taking samples of
  - 18 said incoming data stream in accordance with said first
  - 19 group of sampling clock pulses to produce a first sampled
  - 20 data stream while taking samples of said incoming data
  - 21 stream in accordance with said second group of sampling
  - 22 clock pulses to produce a second sampled data stream;
  - 23 and
  - 24 a phase detection and correction circuit coupled to
  - 25 said data and phase sampling circuit, for determining
  - 26 resemblances of each bit in said second sampled data
  - 27 stream to the corresponding two bits in said first
  - 28 sampled data stream, the associated sampling edge of said
  - 29 bit in said second sampled data stream being adjacent
  - 30 to the associated sampling edges of said two bits in said
  - 31 first sampled data stream, said phase detection and

32 correction circuit producing said phase control signal  
33 on the basis of the resemblance determination result.

1 2. The data recovery circuit of claim 1, wherein said first  
2 sampled data stream is used as a data recovery output.

1 3. The data recovery circuit of claim 1, wherein said first  
2 group of sampling clock pulses and said second group of  
3 sampling clock pulses have the same frequency, which is  
4 equal to half the frequency of said incoming data stream.

1 4. The data recovery circuit of claim 3, wherein said first  
2 group of sampling clock pulses includes a first clock  
3 signal and said second group of sampling clock pulses  
4 includes a second clock signal, said first clock signal  
5 and said second clock signal being 90 degrees out of phase  
6 with each other, and both rising edges and falling edges  
7 of said first clock signal and said second clock signal  
8 being used as said sampling edges.

1 5. The data recovery circuit of claim 3, wherein said first  
2 group of sampling clock pulses includes a first clock  
3 signal and a third clock signal and said second group  
4 of sampling clock includes a second clock signal and a  
5 forth clock signal, said first clock signal and said  
6 second clock signal being 90 degrees out of phase with  
7 each other, said first clock signal and said third clock  
8 signal being 180 degrees out of phase with each other,  
9 and said second clock signal and said forth clock signal  
10 being 180 degrees out of phase with each other.

1 6. The data recovery circuit of claim 5, wherein rising edges  
2 of said first to said forth clock signals are used as  
3 said sampling edges.

1 7. The data recovery circuit of claim 5, wherein falling  
2 edges of said first to said forth clock signals are used  
3 as said sampling edges.

1 8. The data recovery circuit of claim 1, wherein said first  
2 group of sampling clock pulses and said second group of  
3 sampling clock pulses have the same frequency, which is  
4 equal to the frequency of said incoming data stream.

1 9. The data recovery circuit of claim 1, further comprising  
2 a demultiplexer coupled between said data and phase  
3 sampling circuit and said phase detection and correction  
4 circuit, for converting said first sampled data stream  
5 and said second sampled data stream from serial data to  
6 parallel data.

1 10. The data recovery circuit of claim 1, wherein said phase  
2 detection and correction circuit comprises:  
3 an early/late determination circuit for receiving said  
4 first sampled data stream and said second sampled data  
5 stream and determining resemblances of each bit in said  
6 second sampled data stream to the corresponding two bits  
7 in said first sampled data stream, the associated  
8 sampling edge of said bit in said second sampled data  
9 stream being adjacent to the associated sampling edges  
10 of said two bits in said first sampled data stream, said  
11 early/late determination circuit selectively producing  
12 an early signal and a late signal;  
13 an early/late summation circuit for receiving said  
14 early signal and said late signal and producing an  
15 early/late summation signal on the basis of a summation  
16 result of said early signal and said late signal; and

17       a low pass filter for receiving said early/late  
18       summation signal and producing said phase control  
19       signal.

1       11.The data recovery circuit of claim 10, wherein said  
2       early/late determination circuit comprises:

3       a resemblance detection circuit for detecting whether  
4       or not said corresponding two bits in said first sampled  
5       data stream are the same, detecting whether said bit in  
6       said second sampled data stream is equal to the former  
7       or the latter of said corresponding two bits if said two  
8       bits are not the same, and accordingly producing a  
9       resemblance signal of said bit; and

10       an early/late decision circuit for receiving the  
11       resemblance signals of a predetermined number of bits,  
12       comparing the number of times that said bit is equal to  
13       the former of said corresponding two bits with the number  
14       of times that said bit is equal to the latter of said  
15       corresponding two bits, and selectively producing said  
16       early signal or said late signal.

1       12.The data recovery circuit of claim 10, wherein said  
2       early/late summation circuit performs an addition  
3       operation to add one to an accumulative amount responsive  
4       to receiving said early signal while performs an  
5       subtraction operation to subtract one from the  
6       accumulative amount responsive to receiving said late  
7       signal and outputs the accumulative amount as said  
8       early/late summation signal, and wherein said low pass  
9       filter produces said phase control signal on the basis  
10       of the polarity of said early/late summation signal  
11       obtained after a predetermined times of summation  
12       operations by said early/late summation circuit.

1     13. A phase detection circuit for detecting phase conditions  
2         of a first group of sampling clock pulses and a second  
3         group of sampling clock pulses in a data recovery circuit,  
4         said first group of sampling clock pulses being used for  
5         sampling approximately a central portion of each data  
6         bit in an incoming data stream to produce a first sampled  
7         data stream while said second group of sampling clock  
8         pulses being used for sampling approximately a  
9         transition portion between every two data bits in said  
10        incoming data stream to produce a second sampled data  
11        stream, said phase detection circuit comprising:  
12        an early/late determination circuit for receiving said  
13        first sampled data stream and said second sampled data  
14        stream, comprising:  
15        a resemblance detection circuit including a  
16        plurality of resemblance detecting units, each of said  
17        plurality of resemblance detecting units being used for  
18        detecting whether one of a plurality of bits in said  
19        second sampled data stream is equal to the former or  
20        the latter of the corresponding two bits in said first  
21        sampled data stream and producing one of a plurality  
22        of resemblance signals; and  
23        an early/late decision circuit for receiving said  
24        plurality of resemblance signals corresponding to said  
25        plurality of bits, comparing the number of times that  
26        one bit is equal to the former of the corresponding two  
27        bits with the number of times that one bit is equal to  
28        the latter of the corresponding two bits, and  
29        selectively producing an early signal or a late signal.

1     14. The phase detection circuit of claim 13, further  
2        comprising an early/late summation circuit for receiving

3       said early signal and said late signal and producing an  
4       early/late summation signal on the basis of a summation  
5       result of said early signal and said late signal.

1       15. The phase detection circuit of claim 14, wherein said  
2       early/late summation circuit performs an addition  
3       operation to add one to an accumulative amount responsive  
4       to receiving said early signal while performs an  
5       subtraction operation to subtract one from the  
6       accumulative amount responsive to receiving said late  
7       signal and outputs the accumulative amount as said  
8       early/late summation signal.

1       16. A phase detection circuit for detecting phase conditions  
2       of a first group of sampling clock pulses and a second  
3       group of sampling clock pulses in a data recovery circuit,  
4       said first group of sampling clock pulses being used for  
5       sampling approximately a central portion of each data  
6       bit in an incoming data stream to produce a first sampled  
7       data stream while said second group of sampling clock  
8       pulses being used for sampling approximately a  
9       transition portion between every two data bits in said  
10      incoming data stream to produce a second sampled data  
11      stream, said phase detection circuit comprising:

12       an early/late determination circuit for receiving said  
13      first sampled data stream and said second sampled data  
14      stream, said early/late determination circuit  
15      determining a resemblance of said first sampled data  
16      stream and said second sampled data stream by detecting  
17      whether one bit in said second sampled data stream is  
18      equal to the former or the latter of the corresponding  
19      two bits in said first sampled data stream and producing  
20      an early signal or a late signal; and

21 an early/late summation circuit for receiving said  
22 early signal and said late signal and producing an  
23 early/late summation signal on the basis of a summation  
24 result of said early signal and said late signal.

1 17.A data recovery circuit, comprising:  
2 a clock generator for generating a first group of  
3 sampling clock pulses and a second group of sampling  
4 clock pulses for sampling an incoming data stream, each  
5 sampling edge of said first group of sampling clock  
6 pulses and each sampling edge of said second group of  
7 sampling clock pulses being arranged alternatively and  
8 being separated from each other for an interval equal  
9 to half the period of said incoming data stream, said  
10 clock generator being controlled in response to a phase  
11 control signal to adjust phases of said first group of  
12 sampling clock pulses and said second group of sampling  
13 clock pulses;  
14 a data and phase sampling circuit for receiving said  
15 incoming data stream, said first group of sampling clock  
16 pulses and said second group of sampling clock pulses,  
17 said data and phase sampling circuit taking samples of  
18 approximately a central portion of each data bit in said  
19 incoming data stream in accordance with said first group  
20 of sampling clock pulses to produce a first sampled data  
21 stream while taking samples of approximately a  
22 transition portion of every two bits in said incoming  
23 data stream in accordance with said second group of  
24 sampling clock pulses to produce a second sampled data  
25 stream; and  
26 a phase detection and correction circuit coupled to  
27 said data and phase sampling circuit, for determine

28        resemblances of each bit in said second sampled data  
29        stream to the corresponding two bits in said first  
30        sampled data stream, said phase detection and correction  
31        circuit defining an early condition for the phases of  
32        said first group of sampling clock pulses and said second  
33        group of sampling clock pulses if each bit in said second  
34        sampled data stream resembles the former of the  
35        corresponding two bits in said first sampled data stream  
36        while defining a late condition for the phases of said  
37        first group of sampling clock pulses and said second  
38        group of sampling clock pulses if each bit in said second  
39        sampled data stream resembles the latter of the  
40        corresponding two bits in said first sampled data stream,  
41        and producing said phase control signal on the basis of  
42        said early condition or said late condition to adjust  
43        the phases of said first group of sampling clock pulses  
44        and said second group of sampling clock pulses by  
45        shifting the phases backwards or forwards.

1        18. The data recovery circuit of claim 17, wherein said first  
2        sampled data stream is used as a data recovery output.

1        19. The data recovery circuit of claim 17, wherein said first  
2        group of sampling clock pulses and said second group of  
3        sampling clock pulses have the same frequency, which is  
4        equal to half the frequency of said incoming data stream.

1        20. The data recovery circuit of claim 19, wherein said first  
2        group of sampling clock pulses includes a first clock  
3        signal and said second group of sampling clock pulses  
4        includes a second clock signal, said first clock signal  
5        and said second clock signal being 90 degrees out of phase  
6        with each other, and both rising edges and falling edges



7 of said first clock signal and said second clock signal  
8 being used as said sampling edges.

1 21. The data recovery circuit of claim 19, wherein said first  
2 group of sampling clock pulses includes a first clock  
3 signal and a third clock signal and said second group  
4 of sampling clock includes a second clock signal and a  
5 forth clock signal, said first clock signal and said  
6 second clock signal being 90 degrees out of phase with  
7 each other, said first clock signal and said third clock  
8 signal being 180 degrees out of phase with each other,  
9 and said second clock signal and said forth clock signal  
10 being 180 degrees out of phase with each other.

1 22. The data recovery circuit of claim 21, wherein rising  
2 edges of said first to said forth clock signals are used  
3 as said sampling edges.

1 23. The data recovery circuit of claim 21, wherein falling  
2 edges of said first to said forth clock signals are used  
3 as said sampling edges.

1 24. The data recovery circuit of claim 17, wherein said first  
2 group of sampling clock pulses and said second group of  
3 sampling clock pulses have the same frequency, which is  
4 equal to the frequency of said incoming data stream.

1 25. The data recovery circuit of claim 17, further  
2 comprising a demultiplexer coupled between said data and  
3 phase sampling circuit and said phase detection and  
4 correction circuit, for converting said first sampled  
5 data stream and said second sampled data stream from  
6 serial data to parallel data.

1     26. The data recovery circuit of claim 17, wherein said phase  
2       detection and correction circuit comprises:  
3       an early/late determination circuit for receiving said  
4       first sampled data stream and said second sampled data  
5       stream, determining whether each bit in said second  
6       sampled data stream resembles the former or the latter  
7       of the corresponding two bits in said first sampled data  
8       stream, and selectively producing an early signal or a  
9       late signal;  
10      an early/late summation circuit for receiving said  
11      early signal and said late signal and producing an  
12      early/late summation signal on the basis of a summation  
13      result of said early signal and said late signal; and  
14      a low pass filter for receiving said early/late  
15      summation signal and producing said phase control signal  
16      to adjust the phases of said first group of sampling clock  
17      pulses and said second group of sampling clock pulses  
18      by shifting the phases backwards or forwards.

1     27. The data recovery circuit of claim 26, wherein said  
2       early/late summation circuit performs an addition  
3       operation to add one to an accumulative amount responsive  
4       to receiving said early signal while performs an  
5       subtraction operation to subtract one from the  
6       accumulative amount responsive to receiving said late  
7       signal and outputs the accumulative amount as said  
8       early/late summation signal, and wherein said low pass  
9       filter produces said phase control signal on the basis  
10      of the polarity of said early/late summation signal  
11      obtained after a predetermined times of summation  
12      operations by said early/late summation circuit.

1     28. A method for detecting and correcting phase conditions

2 in a data recovery circuit, comprising:  
3 sampling approximately a central portion of each data  
4 bit in an incoming data stream in accordance with a first  
5 group of sampling clock pulses to produce a first sampled  
6 data stream while sampling approximately a transition  
7 portion between every two data bits in said incoming data  
8 stream in accordance with a second group of sampling  
9 clock pulses to produce a second sampled data stream;  
10 detecting whether each bit in said second sampled data  
11 stream resembles the former or the latter of the  
12 corresponding two bits in said first sampled data stream;  
13 summarizing a plurality of detection results produced  
14 in said detecting step to determine whether the phases  
15 of said first group of sampling clock pulses and said  
16 second group of sampling clock pulses are in an early  
17 condition or in a late condition; and  
18 adjusting the phases of said first group of sampling  
19 clock pulses and said second group of sampling clock  
20 pulses by shifting the phases backwards or forwards on  
21 the basis of said early condition or said late condition.

1 29. A method for detecting and correcting phase conditions  
2 in a data recovery circuit, comprising:  
3 sampling approximately a central portion of each data  
4 bit in an incoming data stream in accordance with a first  
5 group of sampling clock pulses to produce a first sampled  
6 data stream while sampling approximately a transition  
7 portion between every two data bits in said incoming data  
8 stream in accordance with a second group of sampling  
9 clock pulses to produce a second sampled data stream;  
10 combining a predetermined number of bits in said first  
11 sampled data stream into a group to form a plurality of

12 first sampled data groups and combining a predetermined  
13 number of bits in said second sampled data stream into  
14 a group to form a plurality of second sampled data groups;  
15 for each first sampled data group and the corresponding  
16 second sampled data group, detecting whether each bit  
17 in said second sampled data stream is equal to the former  
18 or the latter of the corresponding two bits in the first  
19 sampled data stream and respectively counting the number  
20 of times that said bit is equal to the former of said  
21 corresponding two bits and the number of times that said  
22 bit is equal to the latter of said corresponding two bits;  
23 for each first sampled data group and the corresponding  
24 second sampled data group, producing an early signal if  
25 the number of times that said bit is equal to the former  
26 of said corresponding two bits is greater than the number  
27 of times that said bit is equal to the latter of said  
28 corresponding two bits, and producing a late signal if  
29 the number of times that said bit is equal to the latter  
30 of said corresponding two bits is greater than the number  
31 of times that said bit is equal to the former of said  
32 corresponding two bits;  
33 summarizing a plurality of early signals and late  
34 signals to determine whether the phases of said first  
35 group of sampling clock pulses and said second group of  
36 sampling clock pulses are in a early condition or in a  
37 late condition; and  
38 adjusting the phases of said first group of sampling  
39 clock pulses and said second group of sampling clock  
40 pulses by shifting the phases backwards or forwards on  
41 the basis of said early condition or said late condition.

1 30. The method of claim 29, wherein said step of summarizing

2 a plurality of early signals and late signals is carried  
3 out by performing an addition operation to add one to  
4 an accumulative amount responsive to receiving said  
5 early signal while performing an subtraction operation  
6 to subtract one from the accumulative amount responsive  
7 to receiving said late signal and outputting the  
8 accumulative amount as an early/late summation signal.

1 31. The method of claim 30, wherein said step of adjusting  
2 the phases of said first group of sampling clock pulses  
3 and said second group of sampling clock pulses by shifting  
4 the phases backwards or forwards is performed on the basis  
5 of the polarity of said early/late summation signal.